11. (Amended) A semiconductor device manufacturing method for forming a first vertical type high speed NPN bipolar transistor and a second vertical type high voltage NPN bipolar transistor whose breakdown voltage is higher than [different from] that of said first vertical type bipolar transistor on a semiconductor substrate made by forming an epitaxial layer on a silicon substrate, comprising the steps of, before said epitaxial layer is formed on said silicon substrate:

forming in an upper part of said silicon substrate, in a region where said first vertical type bipolar transistor is to be formed, a first embedded diffusion layer of a [the] same conductive type as said epitaxial layer and having an impurity concentration higher than an [the] impurity concentration of said epitaxial layer; and

forming in an upper part of said silicon substrate in a region where said second vertical type bipolar transistor is to be formed, a second embedded diffusion layer of a [the] same conductive type as said epitaxial layer and having an impurity concentration lower than the impurity concentration of said first embedded diffusion layer, said second embedded diffusion layer formed at [and having] a depth deeper than a [the] depth of said first embedded diffusion layer.

Please cancel claims 12-16, without prejudice.

Please add new claims 17 and 18 as follows:

17. A semiconductor device according to claim 1, further comprising:

a third vertical type PNP bipolar transistor having a separating diffusion layer formed in an upper part of said silicon substrate for separating from said silicon substrate a third embedded diffusion layer having an opposite conductive type to said epitaxial layer.

18. A semiconductor device manufacturing method according to claim 11, further comprising the step of:

forming in an upper part of said silicon substrate in a region where a third vertical type PNP bipolar transistor is to be formed a separating diffusion layer for separating from said silicon substrate a third embedded diffusion layer of an opposite conductive type to said epitaxial layer.

REMARKS

In the Office Action dated April 7, 1999, the Examiner rejected claims 1-10 of the present application under 35 U.S.C. §102(b) and/or 35 U.S.C. §103(a) as being anticipated by or, respectively, unpatentable over U.S. Patent No. 4,357,622 to Magdo et al. In light of the above noted amendments, however, Applicants respectfully submit that the claims of the present application, as amended, are both novel and non-obvious over such reference.

Indeed, as noted in the amendment above, the present invention is particularly claimed as a semiconductor device, and method, which includes the specific combination of a high speed NPN bipolar transistor with a high voltage NPN bipolar transistor. Additional specific limitations include a high voltage bipolar transistor breakdown voltage being higher than that of the high speed bipolar

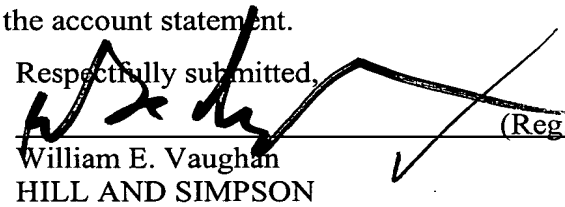
transistor, as well as a second embedded diffusion layer of the high voltage bipolar transistor having an impurity concentration which is less than that of a diffusion layer in the high speed bipolar transistor.

Applicants submit that the combination of a vertical type high speed NPN bipolar transistor with the vertical type high voltage NPN bipolar transistor in the same semiconductor device as claimed in the present invention presents vastly different problems than that which is disclosed in the Magdo reference. To be sure, Magdo merely discloses the combination of complementary, vertical bipolar NPN and PNP transistors on a single semiconductor substrate which have matched high performance characteristics. Such device need not even consider all of the problems associated with combining high speed bipolar transistors with high voltage bipolar transistors in a single device as already discussed, in detail, in the Background of the Invention section of the present application (see, e.g., pages 1-7).

Applicants respectfully submit that none of the references cited by the Examiner, particularly the Magdo reference, either alone or in combination with each other, teach or suggest the specific combination of a first vertical type high speed NPN bipolar transistor with a second vertical type high voltage NPN bipolar transistor on a single semiconductor substrate in a semiconductor device. Accordingly, Applicants respectfully request that the claims as herein proposed be deemed allowable.

It is further submitted that no fees are due in connection with this response at this time. However, if any fees are due in connection with this application, the office is authorized to deduct said fees from Deposit Account No. 08-2290. If such a withdrawal is made, please indicate the Attorney Docket No. (P97,2608) on the account statement.

Respectfully submitted,



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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Assistant Commissioner of Patents Washington, D.C. 20231 on July [illegible], 1999.